THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 53, No. 10, December 1974
Printed in U.S.A.

L5 SYSTEM:

Ultralinear Transistors

By F. A. D'ALTROY, R. M. JACOBS, J. M. NACCI, and E. J. PANNER

(Manuscript received November 9, 1973)

A family of ultralinear npn transistors has been developed for use in the L5 coaxial-carrier system. These 3-GHz devices are characterized by extremely low distortion and noise figure. The transistor comprises an interdigitated base-emitter structure with a heavily doped base grid connected to the peripheral base metal contact. The emitter contact is overlaid on the base-emitter region. Contact metallurgy consists of a platinum silicide, titanium, platinum, and gold system. The transistor is a highly reliable device and meets all the performance requirements of the L5 system.

I. INTRODUCTION

To realize the circuit performance anticipated by raising the coaxial carrier's highest message frequency from the 17.5 MHz of L4 to the 60.5 MHz of L5, it was necessary to develop a new family of npn transistors, the 76 and 77 types. The gain bandwidth product f_T had to be nominally 3,000 MHz; three-tone third-harmonic distortion M_{3E} had to be less than -88 dB below 1 mW and the high-frequency noise figure (NF) kept below 2.4 dB at 30 mA. Power dissipation was to be 1.7 watts, which amounted to a considerable improvement in the state of the art.

The 76-type transistors are used in the equalizing and regulating repeaters and the 77-type in the basic repeater. The 77's are used as matched pairs to lower intermodulation distortion and the noise figure.

One basic design is used to meet all of the equalizer and repeater requirements. Six codes were developed in all, each of which was chosen for a specific purpose, such as low noise for the input stage of the basic repeater, and low distortion for the output stage. Typical characteristics for two codes are given in Table I.

Table I

	77E Typical	77D Typical
$V_{(BR)CEO}$	20	23 V
h_{FE}	100	90
f_T	2200	3000 MHz
NF	2.2	2.7 dB
C_{ob}	3.6	3.6 pF
M_{3E}		−90 dB

II. STRUCTURE

Some carly studies indicated that of the common geometries of power transistors, an interdigitated structure would have the best distortion performance; thus, the present devices are made with interdigitated base and emitter diffusions, hut with an overlaid emitter contact. Base current is carried by the heavily doped base grid, under the overlaid contact, and out to metallized regions at the sides. See Fig. 1. This structure avoids metallizing problems caused by tight metal-contact tolerances, and it minimizes the total area. Emitter bonds are made over the active region, eliminating the emitter pad and its parasitic capacitance. The emitters are 2.5 μm wide and 105 μm long.

The epitaxial thickness is a compromise hetween heing large enough to provide sufficient series collector resistance to minimize second-breakdown problems and yet not so large as to degrade device performance.

III. ENCAPSULATION

Following the practice set hy the L4[1] system, the transistors are encapsulated in a small metal-ceramic package especially designed for rf use. It comprises a kovar-heryllia structure that minimizes parasitic capacitance and lead inductance and provides a relatively low thermal impedance of 30°C/watt. The latter characteristic is important if high reliability and low distortion (see Fig. 2) are to he obtained, since the output transistors in the hasie repeater will operate at 1.7 watts in a peak ambient of 85°C.

IV. DISTORTION

The principal contributor to system noise from the output stage of an amplifier is third harmonic distortion, M_{3E}. In a transistor, this noise arises from two main sources: from the essential nonlinearity of

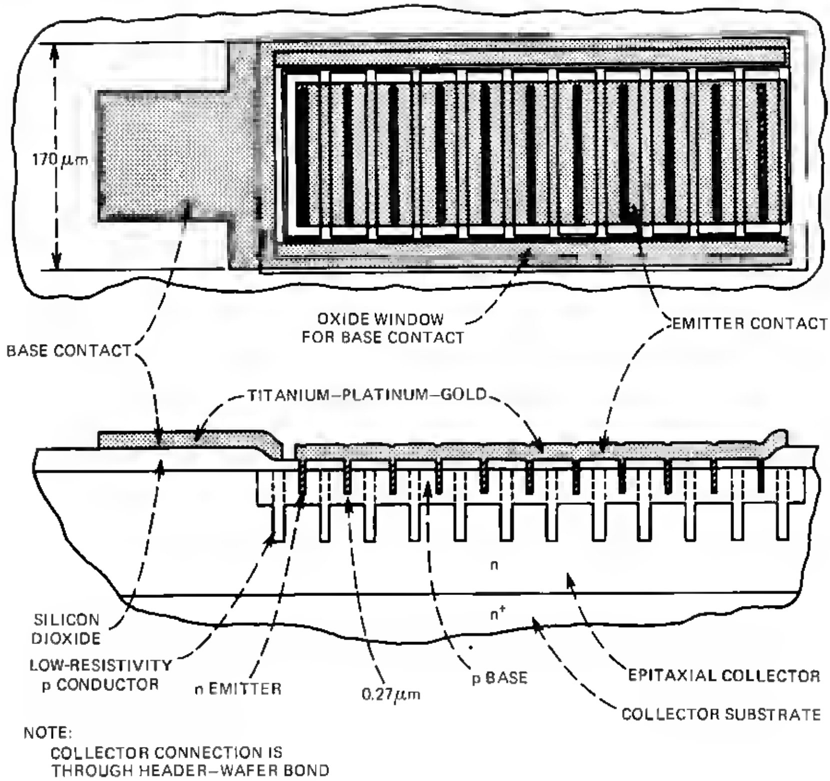

Fig. 1—Structure of L5 transistors.

the emitter current-voltage characteristic and from the falloff of f_T with current[2] owing to conductivity modulation of the collector-junction space-charge region, or Kirk effect.[3] The emitter nonlinearity is the same exponential behavior of the forward-biased diode used, for example, in mixers and for harmonic generation. The nonlinearity is reduced by increasing the total emitter current. Poon[2] has shown that if the emitter area and collector current (effectively the emitter current) are both doubled, M_{3E} decreases by 12 dB (see Fig. 3). If the current density becomes too large, however, distortion arising in the collector starts to degrade the device performance. Whenever the current density exceeds qvN, where q is the electric charge, v the carrier velocity, and N the density of fixed impurities at the collector, the collector-base junction will move in towards the collector substrate and cause f_T to decrease. According to Poon,[2] in the L5 case there is a

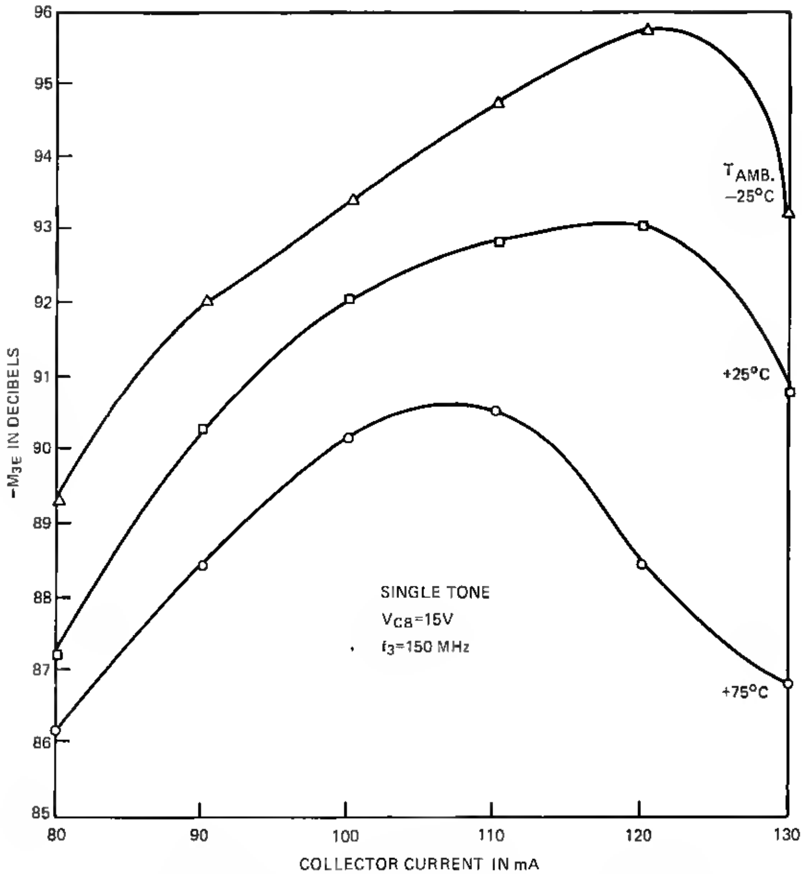

Fig. 2—Temperature dependence of M_{3E} for L5 transistors.

limiting condition given by

$$M_{3E} = -20 \log_{10} \left\{ \frac{R_L 1.2 \times 10^4 \times f_T}{\dfrac{\partial^2 f_T}{\partial I_c^2}} \right\},$$

where R_L is the load resistor and I_c is the collector current.

It can be seen that any mechanism, such as the Kirk effect, which increases the curvature of the f_T vs I_c characteristic, will contribute to harmonic distortion. This means, of course, that as the emitter current is increased to minimize the emitter-distortion term, the collector area must increase proportionately. At some point it ceases to be economic

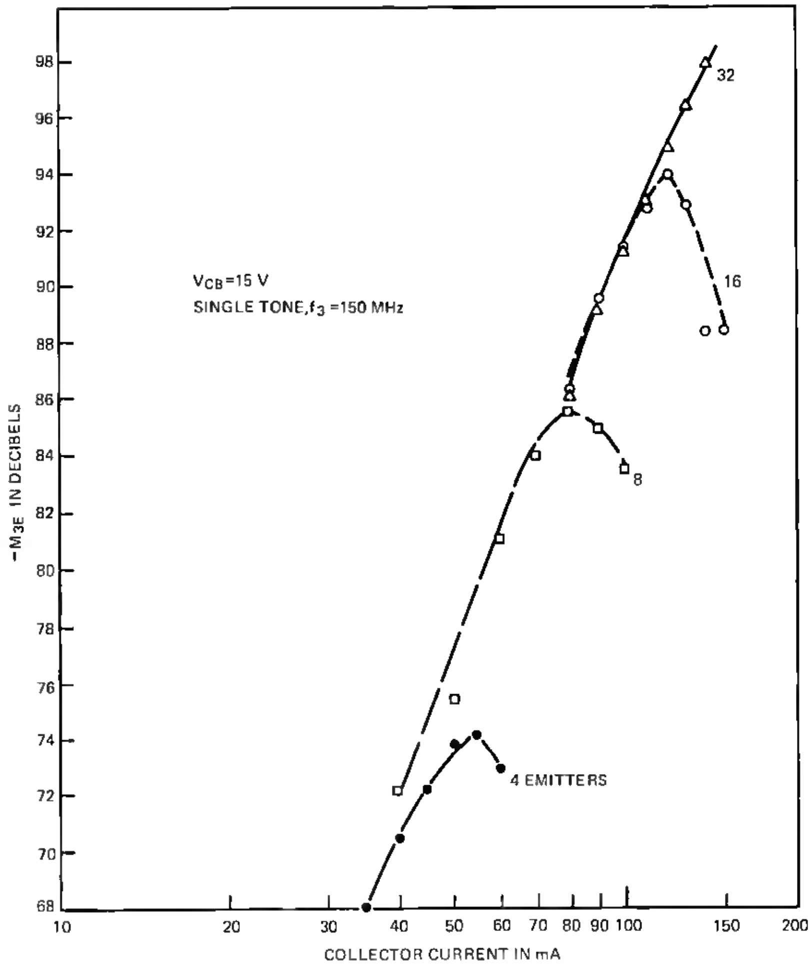

Fig. 3—Harmonic distortion as a function of collector current for several device sizes.

to increase the emitter current because both capacitance and dissipated power become excessive. For the transistor size chosen, a current of 110 mA provides the lowest distortion.

V. SUSTAINING VOLTAGE

The sustaining voltage for the L5 transistor turns out to be bounded at both limits. At the lower limit, it is necessary to keep above the supply voltage, so a value of 18 volts minimum is set. At the upper

limit the doping may become too low and a Kirk effect may occur if the value of the sustaining voltage is made too high. This result can be seen from the following relationships[4]

$$V_{BD} = 1.71 \times 10^9 \left(\frac{N_{BC}}{x_j} \ln \frac{N_o}{N_{BC}} \right)^{-0.364}$$

and

$$V_{CEO} = \frac{V_{BD}}{(\beta)^{1/n}},$$

where

- N_{BC} is the collector epitaxial doping
- N_o is the surface impurity concentration
- x_j is the junction depth
- n is a constant $\simeq 4$ for the transistor concerned.

A practical upper limit is 28 volts.

VI. GAIN BANDWIDTH PRODUCT

One of the basic differences between L4 and L5 transistors is brought about by the increase of the highest message frequency from 17.5 MHz to 60.5 MHz. To accommodate the increased frequency, it is necessary to design the transistor to have a nominal gain bandwidth cutoff, f_T, of 3 GHz. The solution to f_T is given by

$$\frac{1}{2\pi f_T} = \tau_e + \tau_b + \tau_x + \tau_c,$$

where

- τ_e = emitter time constant
- τ_b = base time constant
- τ_x = collector depletion region time constant
- τ_c = collector capacitance time constant.

In the range of large collector-current densities, i.e., $J_c > J_2$,

$$\tau_e = \frac{a_o KT}{qJ_c} C_{te}$$

$$\tau_b \approx \frac{(W_b + W_c)^2}{nD_n} \left\{ 1 - \left[\frac{W_c}{W_b + W_c} \frac{J_2}{J_c} \right]^2 \right\} + \frac{W_b + W_c}{v} \left\{ \frac{J_2}{J_c} \right\} \left\{ 1 - \frac{W_c}{W_b + W_c} \right\} \frac{J_2}{J_c}$$

$$\tau_x \approx 0$$

$$\tau_c \approx 0,$$

where

K = Boltzmann's constant
T = absolute temperature
q = electronic charge
J_c = collector-current density
C_{te} = emitter capacity
W_b = base width
W_c = collector width
D_n = diffusion constant for electrons

$$J_2 = \frac{-V_{cb} + V_o}{\rho_c W_c}$$

V_{cb} = applied voltage
V_o = built-in junction potential
v = carrier velocity

Since τ_b dominates the frequency response, the necessity of keeping the current density low can be readily seen.

Under this condition, τ_b, τ_x and τ_c reduce to

$$\tau_b = \frac{W_b^2}{nD_n} + \frac{W_b}{v_s}$$

$$\tau_x = \frac{X_{mo}}{2v_s}\left\{\frac{1 - J_c/J_2}{1 - J_c/qv_sN_{BC}}\right\}^{\frac{1}{2}}$$

$$\tau_c = \epsilon\rho_c\left\{\frac{W_c}{X_{mo}}\,\frac{1 - J_c/qv_sN_{BC}}{1 - J_c/J_2}\right\}^{\frac{1}{2}},$$

where

v_s = scattering limited velocity
X_{mo} = depletion layer width
ϵ = dielectric constant.

Once the current density has been chosen to be suitably low, the only available design factor for lowering f_T is the actual base width. To achieve an f_T of 3 GHz, it is necessary to lower the base width to 0.27 μm nominal.

VII. NOISE FIGURE

Neilsen's relation[5] for the noise figure, NF, provides a simple means of determining the choice of design parameters for minimizing the noise figure.

$$\mathrm{NF} = 1 + \frac{r_b'}{R_g} + \frac{r_e}{2R_g} + \frac{(1-\alpha_o)\left[1 + \left(\frac{f}{\sqrt{1-\alpha_o}f_\alpha}\right)^2\right](R_g + r_b' + r_e)^2}{2\alpha_o r_e R_g},$$

where

R_g = generator impedance of 50 ohms
r_e = emitter resistance = KT/qI_e
f_α = frequency at which α is 0.707 of its dc value
I_e = emitter current.

It is apparent that once current, gain, and operating frequency have been chosen, r_b' is the only parameter at our disposal and, in fact, for the L5 transistor, the r_b' term is the largest contributor to the noise figure. The term r_b' is made up of two parts. One is the lateral resistance under the emitter stripe, which is minimized by using extremely narrow emitters 2.5 μm in width. The outer component consists of the series resistance to the external base contact. This resistance is reduced to as low a level as possible by the use of a very heavily doped base grid.

VIII. RELIABILITY

During development of the 76- and 77-type transistors, several hundred devices were subjected to accelerated aging of both shelf-temperature and power at junction temperatures up to 300°C. Analysis of the data predicts that the transistors will have a failure rate of considerably less than 10 fits at an operating temperature of 150°C. Under these conditions, it is no longer reliability that is the determinant for system success, but rather, the temperature dependence of the various device parameters.

IX. CONCLUSION

A highly reliable ultralinear family of transistors has been developed for coaxial-carrier-system use. Its high gain-bandwidth product, low noise, and low third-harmonic distortion allow the L5 system to successfully meet its operational requirements with an upper master-group frequency of 60.5 MHz.

REFERENCES

1. N. J. Chaplin, G. A. Dodson, and R. M. Jacobs, "L-4 System: Solid State Devices," B.S.T.J. *48*, No. 4 (April 1969), pp. 983–992.
2. H. C. Poon, "Implication of Transistor Frequency Dependence," IEEE Trans. Electron Devices, *ED-21*, No. 1 (January 1974), pp. 110–112.
3. C. J. Kirk, Jr., "A Theory of Transistor Cutoff Frequency (f_T) Falloff at High Current Densities," IRE Trans. Electron Devices, *ED-9*, No. 2 (March 1962), pp. 164–174.
4. A. B. Phillips, *Transistor Engineering and Introduction to Integrated Semiconductor Circuits*, New York: McGraw-Hill, 1962.
5. E. G. Nielsen, "Behavior of Noise Figure in Junction Transistors," Proc. IRE, *45*, No. 7 (July 1957), pp. 957–963.